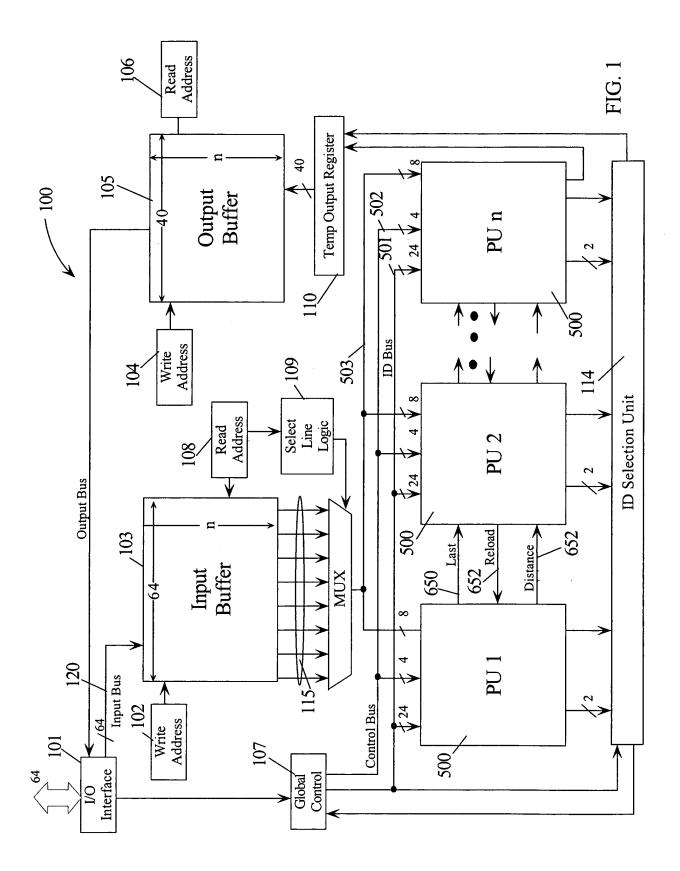
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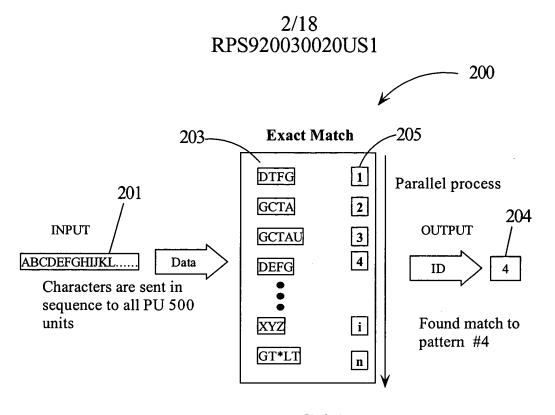


FIG 2A

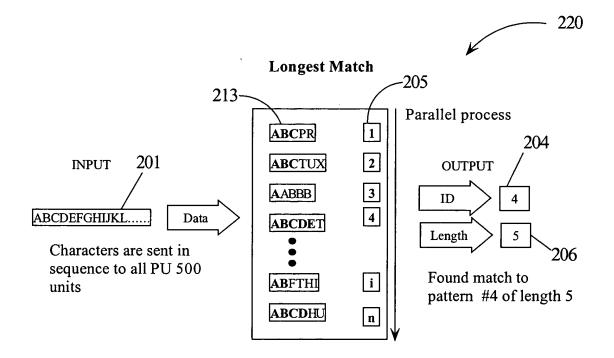


FIG 2B

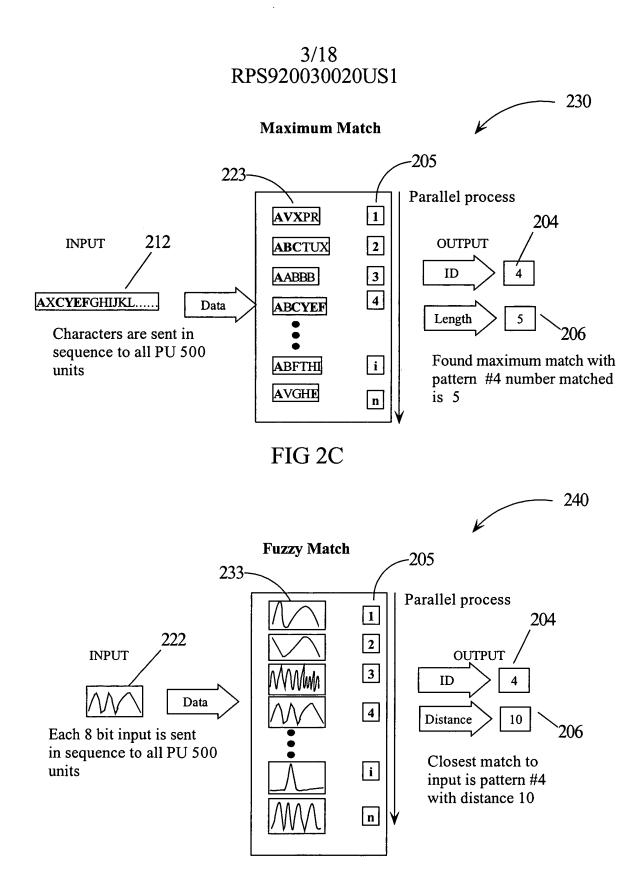


FIG 2D

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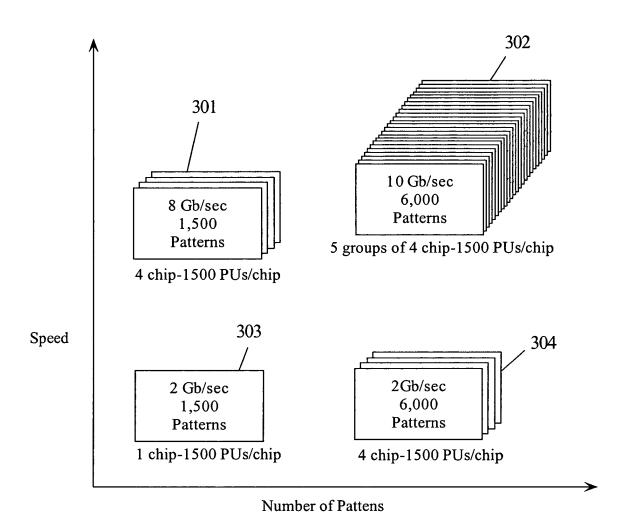
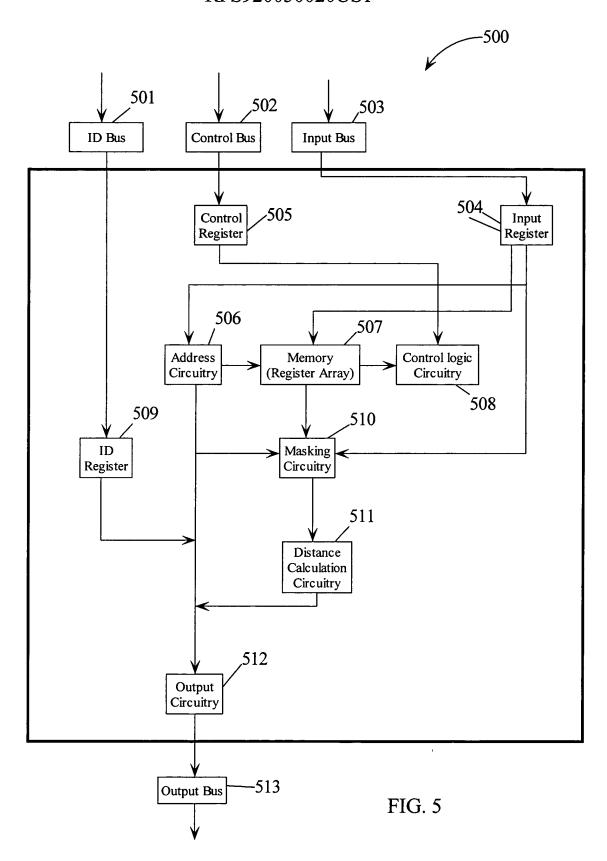


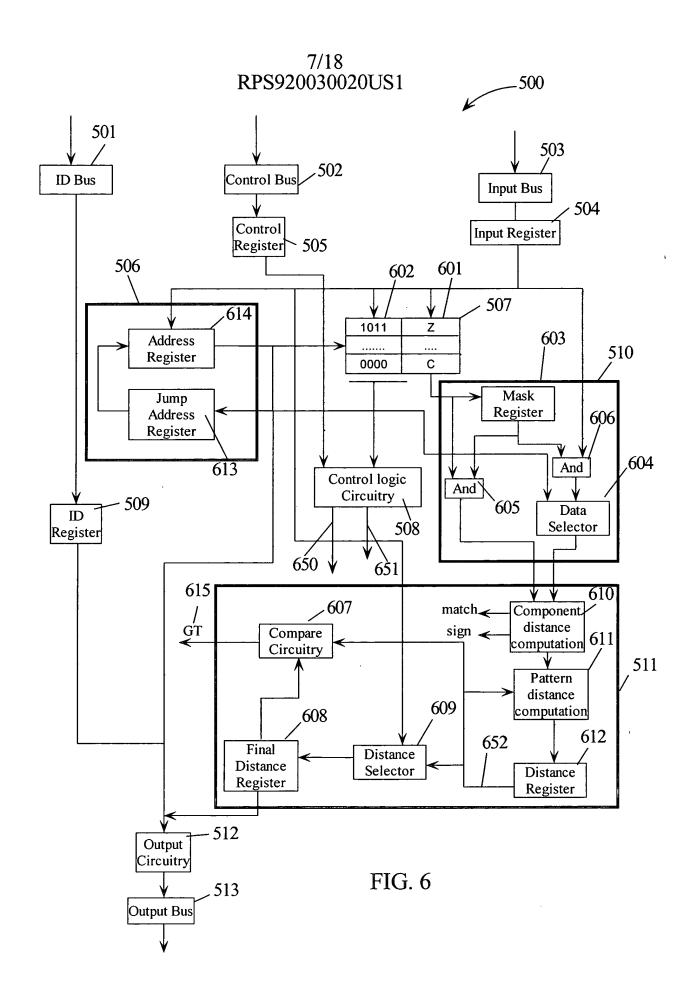
FIG. 3

PPDE 100 Technical Features

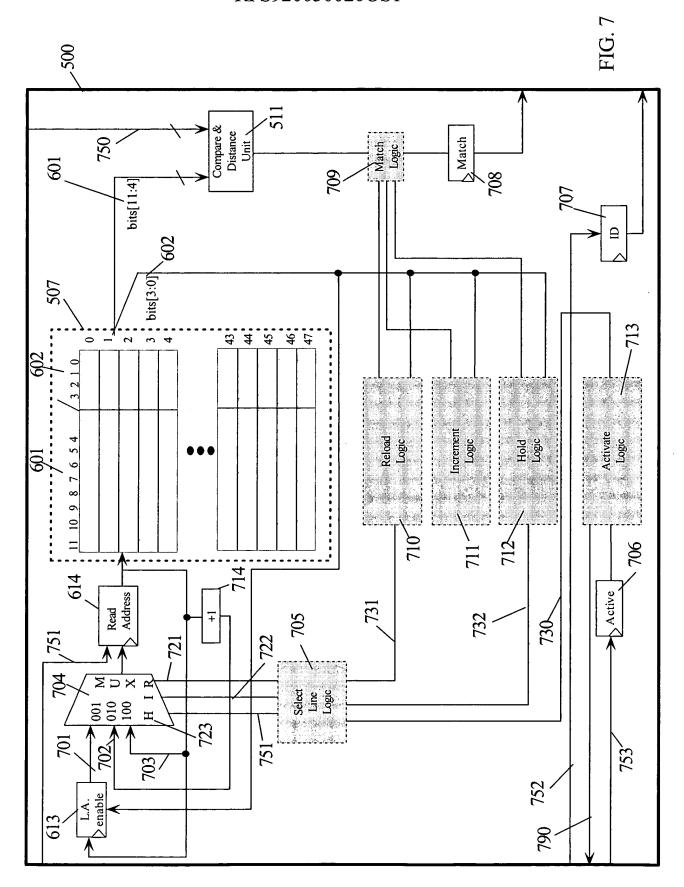
Frequency	0 to 250 MHz
Bandwidth	2Gb/sec at 250 MHz
Compute Power	1.25 TOPS Equivalent
Power Consumption	300mW at 250MHz
Power Supply Vlotage	1.5 V internal (2.5 and 3.3 V compatible)
Technology	CMOS .13 Micron
I/O Pins	88
Die Size	8mm X 8mm
Interface	Fexible interface: max. 64 bits at 66 MHz (max. rate: 4Gb/sec)

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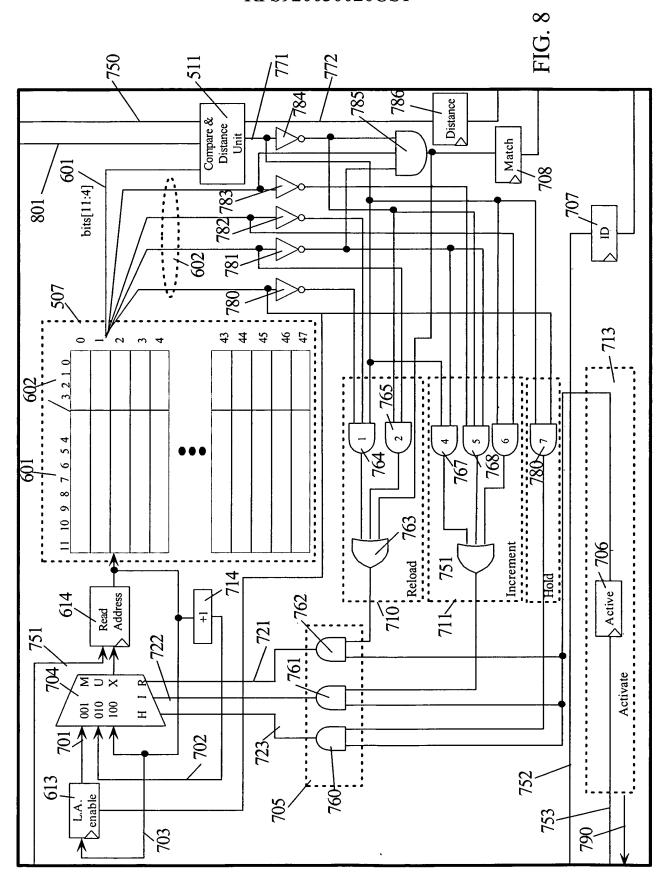




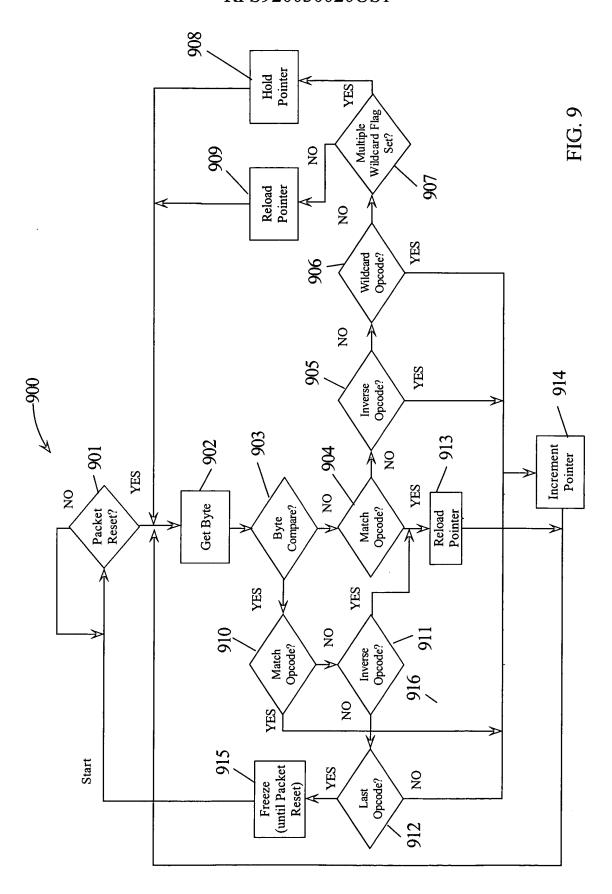
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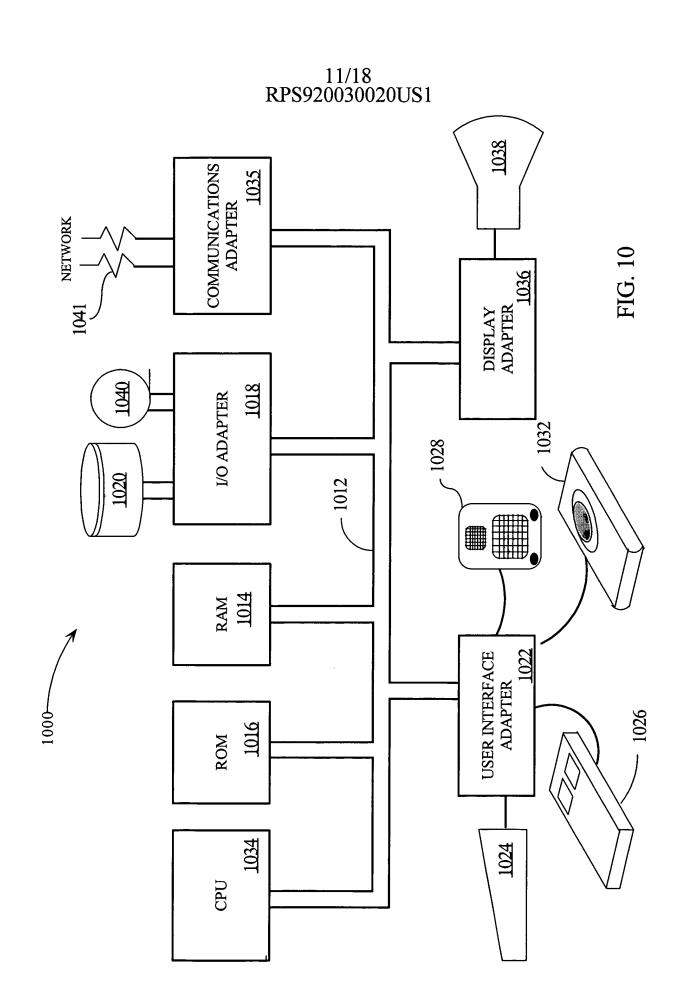


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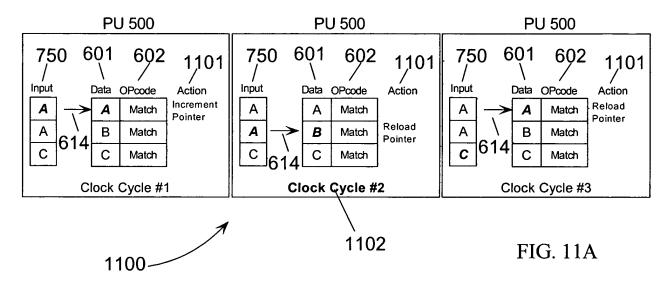


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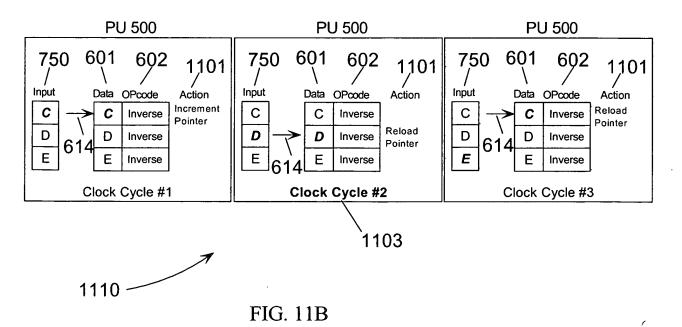




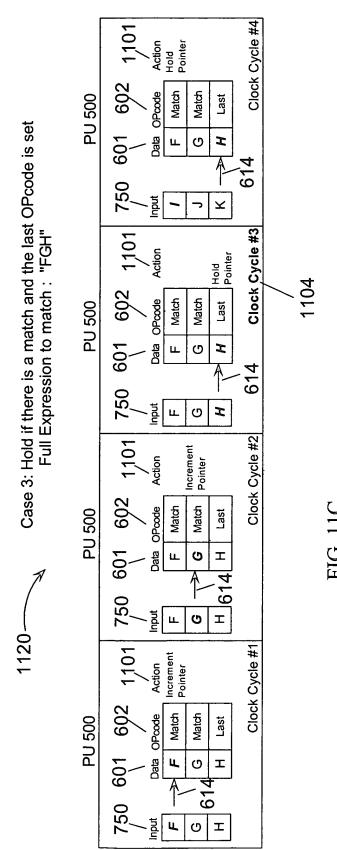
Case 1: Reload if there is NOT a pattern match and the match OPcode is set Partial expression to match: "ABC"



Case 2: Reload if there is a pattern match and the inverse OPcode is set for a pattern byte Partial Expression to match: "C!DE"



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Case 4: Increment if there is NOT a pattern match and the inverse OPcode is set Partial expression to match: "I!LK"

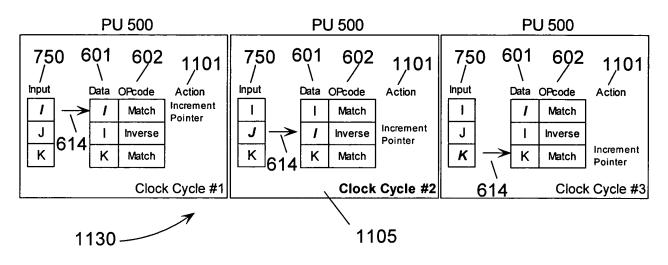


FIG. 11D

Case 5: Increment if there is a pattern match and the match OPcode is set Partial Expression to match: "LMN"

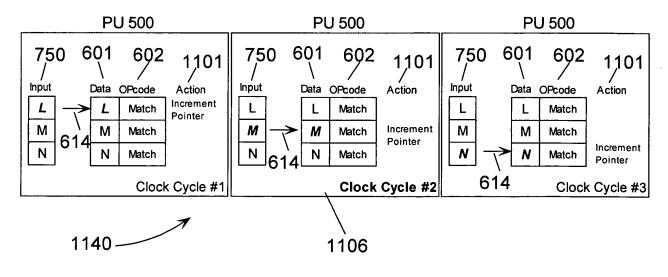


FIG. 11E

Case 6: Increment if there is NOT a pattern match and the wildcard OPcode is set Partial expression to match: "O●Q"

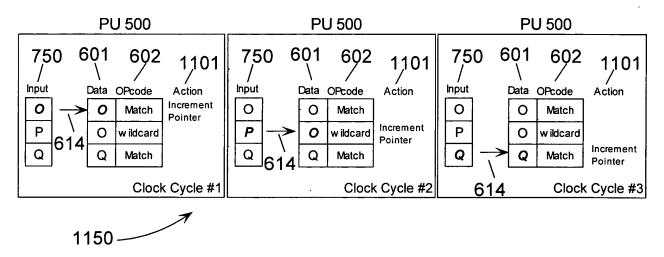


FIG. 11F

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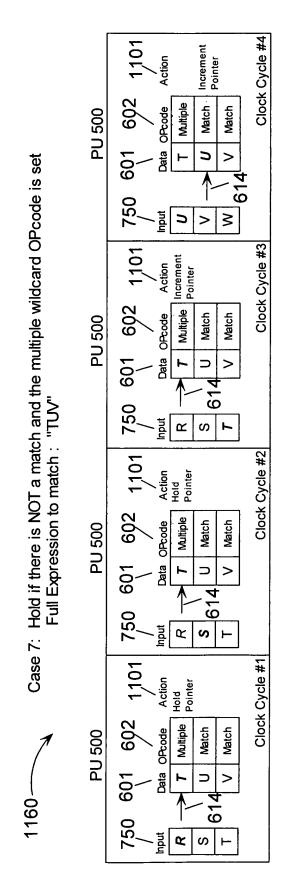


FIG. 11G

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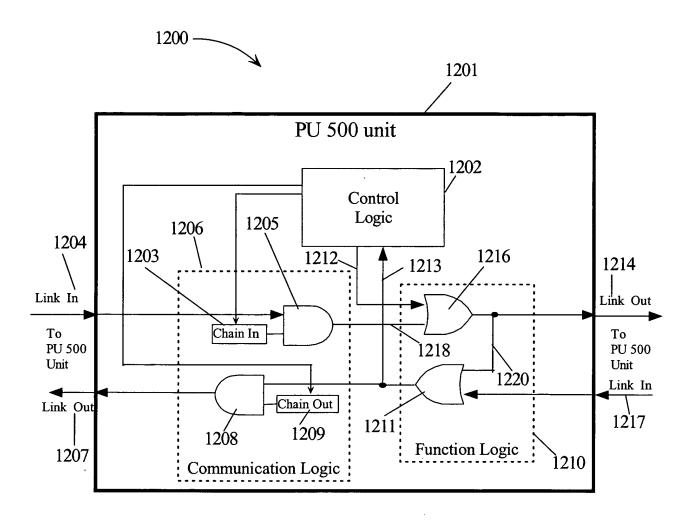


FIG. 12

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